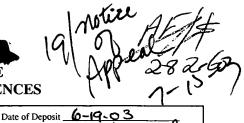


NOTICE OF APPEAL FROM THE PRIMARY EXAMINER TO THE **BOARD OF PATENT APPEALS AND INTERFERENCES**



PATENT APPLICATION

Inventor(S)

Yih-Feng Chyan

August 25, 2000

Case:

15-6-9

Serial No.

Filing Date

09/648164

Group Art Unit: 2826

Dickey

(Signature of person mailing paper or fee)

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I hereby certify that this Norte of Apprilis being deposited with the United State Postal

date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450,

(Printed name of person mailing paper or fee)

Title

Architecture For Circuit Connection Of A Vertical Transistor

Examiner:

ASSISTANT COMMISSIONER FOR PATENTS WASHINGTON, D. C. 20231

SIR:

RECEIVED TC 1700 Applicant(s) hereby appeal(s) to the Board of Patent Appeals and Interferences from the decision dated March 19, 2003 of the Primary Examiner finally rejecting claims: 1, 13, and 14

The item(s) checked below are appropriate:

- [] A Petition for Extension of Time for reply to the rejections is attached.
- Please charge the amount of \$330.00 covering the Appeal Fee (37 CFR 1.17(2)), [X] to Agere Systems Deposit Account No. 501735. Duplicate copy of this letter is enclosed.
- [] Appeal Fee not required. (Fee was paid in prior Appeal.)

In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 501735** as required to correct the error.

Please address all correspondence to Docket Administrator, Agere Systems Inc., 4 Connell

Drive, Room 4U-533C, Berkeley Heights, NJ 07922-2747

06/25/2003 DTESSEM1 00000069 501735

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320.00 DA

Attorney for Applicant(s), Reg. No. 32752

Date: 19 2003